6-V to 30-V Input Voltage, 3-A Output Current, Synchronous Buck LED Driver With PWM Dimming

GERNAL DESCRIPTION

The NS2403 is a 3-A synchronous buck LED driver with 30-V maximum input voltage. By integrating the high-side and low-side NMOS switches, the NS2403 device provides high power density with high efficiency in an ultra-small solution size.
The NS2403 device uses peak-current-mode control and full internal compensation to provide high transient response performance over a wide range of operating conditions.
NS2403 implements PWM dimming mode. In PWM dimming mode, LEDs turn on and off according to PWM duty cycle periodically. For safety and protection, the NS2403 implement full protections, including LED open, LED+ short-to-GND, LED short, sense resistor open and short, and device thermal protection.

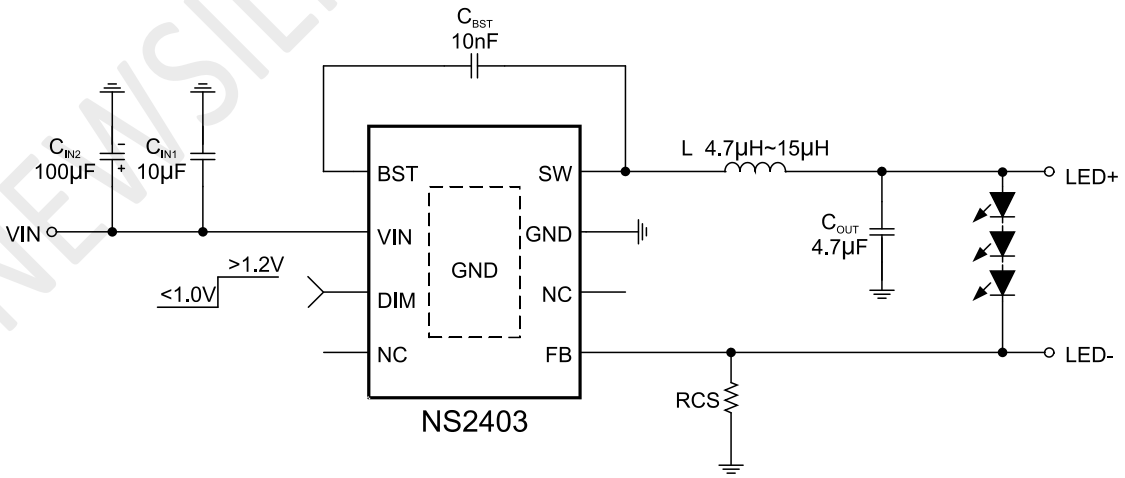
FEATURES

- Wide Input Voltage Range: 6V ~ 30V
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 90mΩ/65 mΩ
- 3-A continuous output current
- PWM dimming with digital input
- 500kHz Switching Frequency Minimize the External Components
- Ultra-low and accurate FB voltage: 99 mV ±3 mV
- Peak current mode with internal compensation
- Compact Package: ESOP8
- Protection
  LED open-load protection
  Over Voltage Protection(OVP)
  LED+ short-to-GND protection with auto-retry
  LED+ and LED– short circuitry protection with auto-retry
  Sense-resistor open-load and short-to-GND protection with auto-retry
  Thermal shutdown protection with auto-retry

APPLICATION

- Video surveillance IR/White LED driver
- Facial recognition IR LED driver
- Stage lighting LED driver
- General industrial and commercial illumination
- Medical UV LED driver

TYPICAL APPLICATIONS



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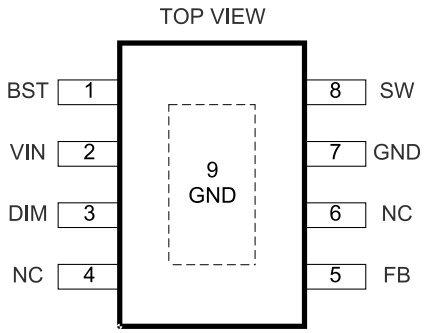
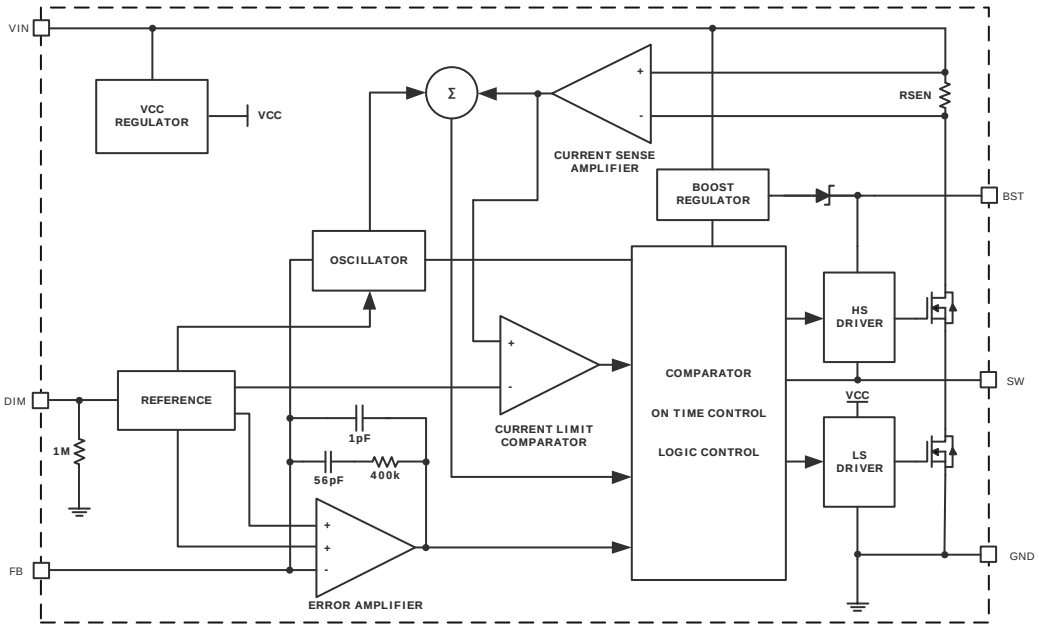
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	BST	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to SW pin with10nF ceramic cap.
2	VIN	Supply Voltage. The NS2403 operates from a 6V to 30V input rail. Requires C_{IN} to decouple the input rail. Connect using a wide PCB trace.
3	DIM	Dimming input. In PWM dimming mode, LED current is turned ON and OFF according to PWM duty cycle periodically
4	NC	NC
5	FB	LED current detection feedback
6	NC	NC
7	GND	System Ground. Reference ground of the regulated output voltage: requires extra care during PCB layout. Connect to GND with copper traces and vias.
8	SW	Switch Output. Connect using a wide PCB trace.
9	GND	EPAD, connect to GND

SYSTEM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNIT
Supply Input Voltage	-0.3	38	V
SW,DIM Voltage	-0.3	V_{IN} + 0.3	V
FB, BS-SW Voltage	-0.3	4	V
Junction Temperature Range	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	°C
Storage Temperature Range	-65	150	°C
Dynamic SW Voltage in 10ns Duration	GND-5V	V_{IN}+3V	V
Power Dissipation, PD @ TA = 25°C TSOT23-6		2	W
Package Thermal Resistance θ_{JA}		105	°C/W
Package Thermal Resistance θ_{JC}		55	°C/W
HBM(Human Body Mode)		2	kV
MM(Machine Mode)		200	V

ESD(electrostatic discharge) sensitive device.
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
Supply Input Voltage	6	30	V
Junction Temperature Range	-40	150	°C
Ambient Temperature Range	-40	85	°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{OUT} = 5V, L = 10μH, C_{OUT} = 44μF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}		6		30	V
Input OVP Threshold	V_{OVP}				30	V
Input OVP Hysteresis	V_{HYS}			3		V
Input UVP Threshold	V_{UVP}				5.3	V
Input UVP Hysteresis	V_{HYS}			0.6		V
Standby Supply Current	I_Q	V_{DIM}=2V,V_{FB}=0.105V		110		μA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0		2		μA
EN Rising Threshold	V_{EN_R}			1.2		V
EN Falling Threshold	V_{EN_F}			1		V
Feedback Voltage	V_{REF}		94	100	106	mV
Top FET RON	R_{DSON}			90		mΩ
Bottom FET RON	R_{DSON}			65		mΩ
Min ON Time	T_{ON_MIN}			80	100	ns
Min OFF Time	T_{OFF_MIN}			80	100	ns
Max Duty Cycle				85%		
Switching Frequency	F_{SW}			500		kHz
Top FET Current Limit	I_{LIM_TOP}			3.5		A
Bottom FET Current Limit	I_{LIM_BOT}			3.5		A
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

GENERAL DESCRIPTION

Feature Description

The NS2403 device is a 3-A synchronous buck LED driver with 30-V maximum input voltage. By integrating the high-side and low-side NMOS switches, the NS2403 device provides high power density with high efficiency in an ultra-small solution size.

The NS2403 device is fully internally compensated without additional external components, which enables a simple design on a limited board space. The device uses peak current mode control to regulate the LED current with high accuracy. Switching frequency is internally set to 500kHz, allowing the use of extremely small surface-mount inductors and chip capacitors.

The NS2403 devices support PWM dimming mode. In PWM dimming mode, the LED turns on and off according to PWM duty cycle periodically.

For safety and protection, the NS2403 implement full protections include LED open, LED+ short-to GND, LED short, sense resistor open and short, and device thermal protection. Hiccup mode is triggered at current limit or FB pin overvoltage scenario to avoid the device overheats

Input UVP

The device implements internal Under voltage Protection (UVP) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVP threshold, 5.3-V typical. The internal IN UVP threshold has a hysteresis of 0.6-V typical.

Input OVP

The device implements internal Over voltage Protection (OVP) circuitry on the VIN pin. The device is disabled when the VIN pin voltage rises over the internal VIN OVP threshold, 30-V typical. The internal IN OVP threshold has a hysteresis of 3-V typical.

Dimming and Enable/Disable

When the input voltage is above maximal UVP rising threshold and the DIM pin is pulled high (above 1.2V), the NS2403 is enabled. When the DIM pin is pulled low (below 1V), the NS2403 goes into shutdown mode. In shutdown mode, less than 1μA input current is consumed. The DIM pin allows disabling and enabling of the device as well as brightness control of the LEDs by applying a PWM signal. When a PWM signal is applied, the LED current is turned on when the DIM is high and off when DIM is pulled low. Changing the PWM duty cycle therefore changes the LED brightness. When dimming is not needed, we can connect DIM and VIN through a resistor

Peak Current Limit Mode

The NS2403 has both a peak current limit mode and a valley current limit mode to protect the chip from overcurrent damage. The device implements current-mode control, which uses the internal COMP voltage to control the turnoff of the high-side MOSFET and the turn-on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference, the high-side switch turns off. During overcurrent conditions, such as when the sensing resistor is shorted, or an open circuit occurs in the feedback-filter RC network that drives FB low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch-current limit. This current limit is fixed at 3.5A (typical).

Valley Current Limit

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. If the low-side sourcingcurrent limit is exceeded, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the low-side current is below the low-side sourcing currentlimit at the start of a cycle.

LED-Open

When the LED load is open, the FB voltage is low, and the internal COMP voltage is driven high and clamped, then output rises close to the input. At this time, the chip does not have load capacity.

LED Short Protection

When LED+ and LED- are shorted, the output current will be limited to near VFB/RCS. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold. Once a UV is triggered, the NS2403 enters hiccup mode to periodically restart the part. At this time, the output voltage is close to VFB.

LED+ Short to GND Protection

When the LED+ is shorted to GND, the FB voltage is higher than VREF, and the internal COMP voltage is driven low and clamped, and the high-side MOSFET is commanded on for a minimum on-time each cycle.

The device enters fold-back mode, meanwhile, chip reaches internal current limit.

Efficiency and Feedback Voltage

The feedback voltage has a direct effect on the converter efficiency. Because the voltage drop across the feedback resistor does not contribute to the output power (LED brightness), the lower the feedback voltage, the higher the efficiency. Especially when powering only three or less LEDs, the feedback voltage impacts the efficiency around 2% depending on the sum of the forward voltage of the LEDs.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

Detailed Design Procedure

Setting the LED Current

The LED current is controlled by the feedback resistor, RS1, in the following table. The current through the LEDs is given by the equation 100mV/RCS. Following table shows the selection of resistors for a given LED current.

I_{LED}(A)	R_{CS}(ohm)
3	0.033
1.5	0.067
0.1	1

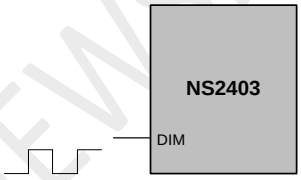
$R_{CS}=0.1/I_{LED}$

I_{LED} is average LED current.

LED Dimming Control

※Using a PWM Signal to EN Pin

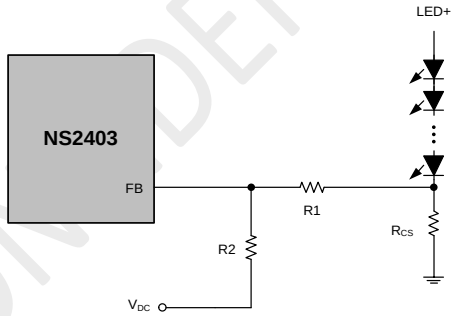
For controlling the LED brightness, the NS2403 can perform the dimming control by applying a PWM signal to EN pin. The internal soft start and the wide range dimming frequency can eliminate inrush current and audio noise when dimming. The average LED current is proportional to the PWM signal duty cycle. The magnitude of the PWM signal should be higher than the maximum enable voltage of DIM pin.



※Using a DC Voltage

Using a variable DC voltage to adjust the brightness is a popular method in some applications. According to the Superposition Theorem, as the DC voltage increases, the voltage contributed to VFB increases and the voltage drop on R1 decreases, i.e. the LED current decreases. For example, if the VDC range is from 0V to 2.8V, the selection of resistors sets dimming control of LED current from 1.5A to 0A.The LED current can be calculated by the following equation:

$$I_{LED} = \frac{V_{FB} - \frac{R1 \times (V_{DC} - V_{FB})}{R2}}{R_{CS}}$$

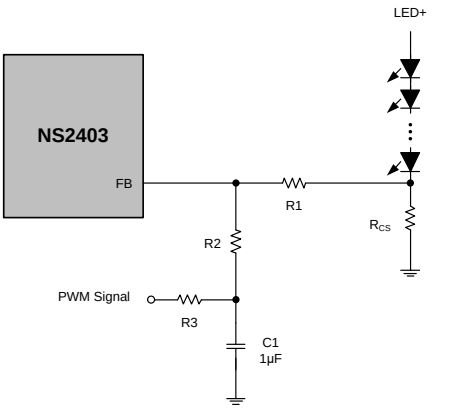


※Using a Filtered PWM signal

Another common application is using a filtered PWM signal as an adjustable DC voltage for LED dimming control. A filtered PWM signal acts as the DC voltage to regulate the output current.Output ripple depends on the frequency of PWM signal. For smaller output voltage ripple (<100mV), the recommended frequency of 2.8V PWM signal should be above 10kHz. To fix the frequency of PWM signal and change the duty cycle of PWM signal can get different output current.

The LED current can be calculated by the following equation:

$$I_{LED} = \frac{V_{FB} - \frac{R1 \times (V_{PWM} \times Duty - V_{FB})}{R3 + R2}}{R_{CS}}$$



Inductor Selection
Select the appropriate inductance value according to different number of series lamp groups. For most applications, 4.7 to 10μH are recommended. Small size and better efficiency are the major concerns for portable device, such as
NS2403 used for mobile phone. When selecting the inductor, the inductor saturation current should be rated as high as the peak inductor current at maximum load, and respectively, maximum LED current.

Input Capacitor Selection
For good input voltage filtering, low ESR ceramic capacitors are recommended. A 10μF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering and EMI reduction, this value can be increased. The input capacitor should be placed as close as possible to the input pin of the converter.

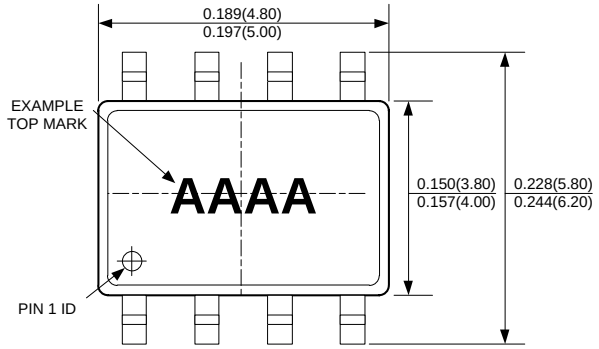
Output Capacitor Selection
The device is designed to operate with a wide selection of ceramic output capacitors. The selection of the output capacitor value is a trade-off between output voltage ripple and capacitor cost and form factor. In general, capacitor values of 4.7μF up to 22μF can be used. For better voltage filtering, ceramic capacitors with low ESR are recommended.
X5R and X7R types are suitable because of their wider voltage and temperature ranges.

Bootstrap Capacitor Selection
Connect a 10nF ceramic capacitor between the SW and BS pins for proper operation. recommends using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 6.3V or higher voltage rating.

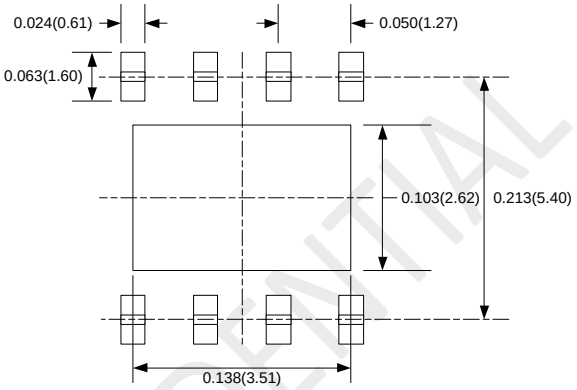
Layout Guidelines
PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.
1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator V_{IN} terminal, to the regulator SW terminal, to the inductor then out to the output capacitor C_{OUT} and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to C_{OUT} and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the V_{IN} terminal. Grounding for both the input and output capacitors should consist of a small localized top side plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

PACKAGE

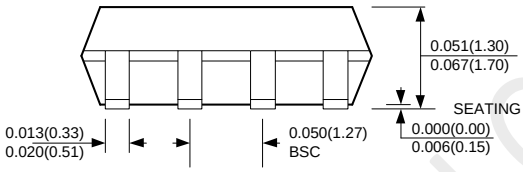
SOP8(EXPOSED PAD)



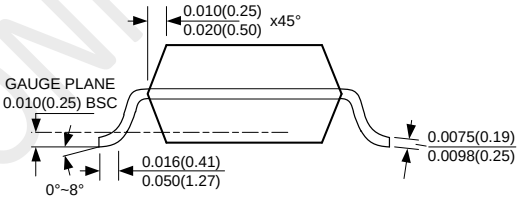
TOP VIEW



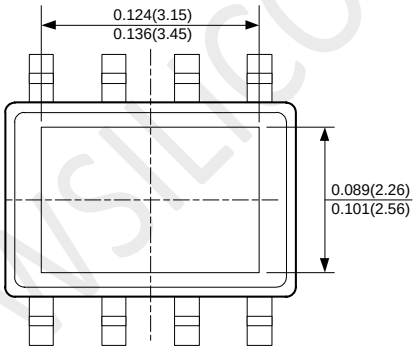
RECOMMENDED SOLDER PAD LAYOUT



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTE:
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.